TTμL 9020

DUAL JK$\overline{K}$ FLIP-FLOP

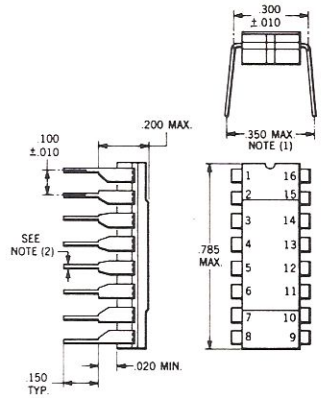
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION

The 9020 consists of two JK flip-flops with a common clock, separate J, K, and $\overline{K}$ inputs and a common JK input. The JK$\overline{K}$ design allows the 9020 to be operated as a D type flip-flop or as a standard J-K flip-flop. Incorporated in the element is a single clock buffer which reduces clock loading.

The joint (JK) input to the flip-flops can be used to advantage for gating information into the flip-flops. This common input removes the necessity of gating clock waveforms and can result in an improved logic design requiring fewer circuits. It also minimizes clock skew problems if a single clock line is used and all the clock drivers are tied together.

PHYSICAL DIMENSIONS



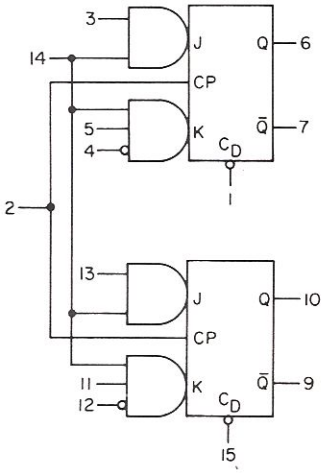
NOTES:

1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES

- **50 MHz operation**
- **Master-slave circuit**
- **Common buffered clock input**
- **Separate JK$\overline{K}$ inputs**
- **Common Input Enable logic**
- **Separate Direct Clear inputs**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL, and MSI families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line package**
- **Input Diode Clamping**

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +8V
Input Voltage	−1.5V to +5.5V
Voltage Applied to Outputs	−0.5V to V_{CC} Value
Current Into Output When Output is Low	50 mA

ORDER INFORMATION

Specify U6B9020XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

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TRUTH TABLE

SYNCHRONOUS ENTRY J-K MODE OPERATION

INPUTS @ t_n			OUTPUTS @ t_{n+1}	
JK 14	J 3(13)	K • $\overline{K}$ 5(11) • 4(12)	Q 6(10)	$\overline{Q}$ 7(9)
L	X	X	(1)	No Change
H	L	L	(1)	No Change
H	L	H	L	H
H	H	L	H	L
H	H	H	Toggles	

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS	OUTPUTS	
C_D 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H
H	No Change	

H = Most positive logic level
L = Most negative logic level
X = Could be high or low

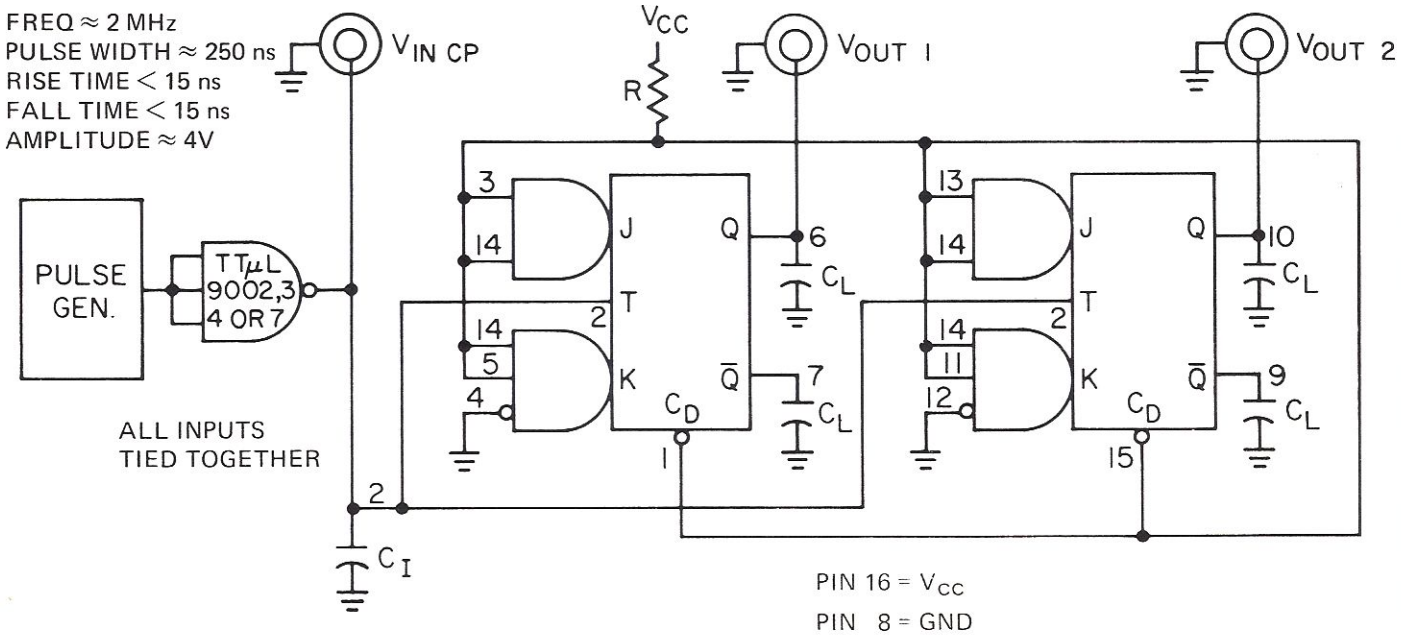
NOTES:

(1) For no change of outputs, the J and K inputs or the common JK input must remain low for the entire period in which the clock pulse is at low logic level.
(2) $\overline{K}$ inputs should be grounded when not in use.

LOADING RULES

INPUTS	LOADING
J, K, $\overline{K}$	1
CP	2
JK	4
CD	2.7
OUTPUTS	**FANOUT**
Q, $\overline{Q}$	10

SWITCHING TIME TEST CIRCUITS:



ELECTRICAL CHARACTERISTICS

INDUSTRIAL TEMPERATURE RANGE 0°C to 75°C, V_{CC} 5.0V ±5%

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75V, I_{OH} = 1.2 mA	
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 4.75V, I_{OL} = 14.1 mA V_{CC} = 5.25V, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs.	
I_R $2\,I_R$ $4\,I_R$ I_{RS}	J, K, $\overline{K}$ Leakage Current Clock Input J-K Input Asynchronous Inputs				5 10 20 14	60 120 240 160		60 120 240 160	μA	V_{CC} = 5.25V, V_R = 4.5V Gnd. on other inputs.	
I_F $2\,I_F$ $4\,I_F$ I_{FSI}	J, K, $\overline{K}$ Input Current Clock Input J-K Input Asynchronous Inputs		−1.60 −3.20 −6.40 −4.32		−1.0 −2.0 −4.0 −2.7	−1.60 −3.20 −6.40 −4.32		−1.60 −3.20 −6.40 −4.32	mA	V_{CC} = 5.25V	V_F = 0.45V V_R = 4.5V on other inputs.
I_F $2\,I_F$ $4\,I_F$ I_{FSI}	J, K, $\overline{K}$ Input Current Clock Input J-K Input Asynchronous Inputs		−1.41 −2.82 −5.64 −3.78		−0.94 −1.88 −3.76 −2.54	−1.41 −2.82 −5.64 −3.78		−1.41 −2.82 −5.64 −3.78	mA	V_{CC} = 4.75V	
t_{pd+}					13	22			ns		V_{CC} = 5.0V
t_{pd-}					21	35			ns		C_L = 15 pF
$t_{release}$					6	1			ns		
$t_{set\text{-}up}$				12	7				ns		
	Negative Clock pulse width			16	11				ns	Toggle Condition	

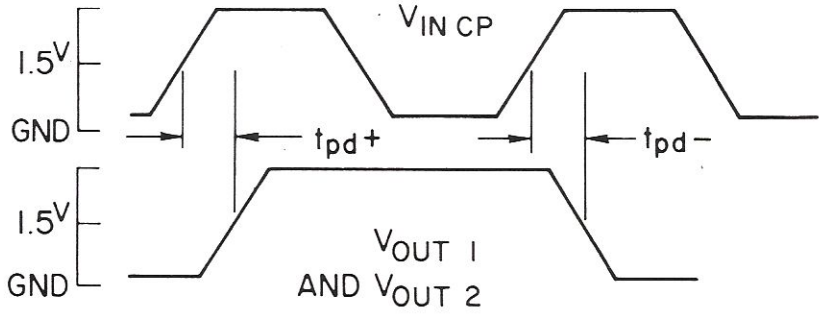
SWITCHING TIME TEST CIRCUITS (Continued)

NOTES:

R = 2K, ±5%, ½W
C_I = 15 pF ±5%
C_L = 15 pF ±5%

C_I & C_L include all probe and jig capacity.
Very short stranded or printed wire should be used for all interconnections.
Probes should be connected directly to the input & output pins.

WAVEFORMS



ELECTRICAL CHARACTERISTICS

MILITARY TEMPERATURE RANGE **–55°C to +125°C, V_{CC} 5.0V ±10%**

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS & COMMENTS	
		–55°C		25°C			125°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5V, I_{OH} = 1.2 mA	
V_{OL}	Qutput Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 12.4 mA V_{CC} = 5.5V, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.	
I_R $2\ I_R$ $4\ I_R$ I_{RS}	J, K, $\overline{K}$ Leakage Current Clock Input J-K Input Asynchronous Inputs				5 10 20 14	60 120 240 160		60 120 240 160	μA	V_{CC} = 5.5V, V_R = 4.5V Gnd. on other inputs.	
I_F $2\ I_F$ $4\ I_F$ I_{FSI}	J, K, $\overline{K}$ Input Current Clock Input J-K Input Asynchronous Inputs		–1.60 –3.20 –6.40 –4.32		–1.1 –2.2 –4.4 –3.0	–1.60 –3.2 –6.40 –4.32		–1.60 –3.2 –6.40 –4.32	mA	V_{CC} = 5.5V	V_F = 0.4V V_R = 4.5V
I_F $2\ I_F$ $4\ I_F$ I_{FSI}	J, K, $\overline{K}$ Input Current Clock Input J-K Input Asynchronous		–1.24 –2.48 –4.86 –3.29		–0.91 –1.82 –3.64 –2.48	–1.24 –2.48 –4.96 –3.29		–1.24 –2.48 –4.96 –3.29	mA	V_{CC} = 4.5V	on other inputs
t_{pd+}					13	22			ns	Each Flip-Flop	V_{CC} = 5.0V
t_{pd-}					21	35			ns		C_L = 15 pF
$t_{release}$					6	1			ns		
$t_{set\text{-}up}$				12	7				ns		
	Negative Clock pulse width			16	11				ns	Toggle Condition	

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